

TABLE 1

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
1	1	RA0	ST		N/A	Port Input
		AN0	AN		—	ADC Input
		OPA+	AN		—	Op Amp Non-inverting Input
2	2	RA1	ST		N/A	Port Input
		AN1	AN		—	ADC Input
		OPA-	AN		—	Op amp Inverting Input
7	7	RA2	ST		CMOS	Bi-directional I/O
		AN2	AN		—	ADC Input
		Vref2	AN		—	Voltage Reference Input for C2 Comparator
8	8	RA3	ST		CMOS	Bi-directional I/O
		AN3	AN		—	ADC Input
		Vref1	AN		—	Voltage Reference Input for C1 Comparator, ADC, and DAC Modules
3	3	RA4	ST		OD	Bi-directional I/O
		T0CKI	ST		—	T0 Clock Input
4	4	RA5	ST		—	Port Input
		MCLR	ST	No	—	Master Clear Input
		Vpp	Power		—	Programming Voltage
17	17	RA6	ST		CMOS	Bi-directional I/O
		OSC2	—		Xtal	Crystal/Resonator
		CLKOUT	—		CMOS	Internal Clock (Fosc/4) Output
18	18	RA7	ST		CMOS	Bi-directional I/O
		OSC1	Xtal		—	Crystal/Resonator
		CLKIN	ST		—	External Clock Input Connection.
		T0CKI	ST		—	Timer1 External Clock Input

TABLE 1 (cont'd)

20 Pin PDIP, SOIC	20 Pin SSOP	Name	Input Type	Pull-up/ Current Source	Output Type	Description
9	9	RB0	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		INT	ST		—	Interrupt
		AN4	AN		—	ADC, C1, or C2 Comparator Input
		VREF			AN	VREF Reference Output
10	10	RB1	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN5	AN		—	ADC, C1, or C2 Comparator Input
		VDAC			AN	DAC Output
19	19	RB2	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN6	AN		—	ADC, C1, or C2 Comparator Input
20	20	RB3	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		AN7	AN		—	ADC, C1, or C2 Comparator Input
		OPA			AN	Op Amp Output
11	11	RB4	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
12	12	RB5	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
13	13	RB6	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1A C1			CMOS	PSMC1A Output
					CMOS	C1 Comparator Output
14	14	RB7	TTL	RBPU	CMOS	Bi-directional I/O with Selectable Pull-up and Interrupt on Change
		PSMC1B C2			CMOS	PSMC1B Output
					CMOS	C2 comparator Output
		T1G	ST		—	Timer1 Gate Input
16	16	Vdd	Power		—	Digital Power
5	5	Vss	Power		—	Digital Ground
15	15	AVdd	Power		—	Analog Power
6	6	AVss	Power		—	Analog Ground

Legend: ST=Schmitt Trigger Input Voltage Levels, CMOS=Complimentary Metal Oxide Semiconductor Output Voltage Levels, TTL=Transistor Transistor Logic Input Voltage Levels, AN=Analog I/O Voltage Levels, OD=Open Drain Output, Xtal=Crystal, RBPU=Port B Pull-Up

TABLE 2A

Alternate Function	PORTA (when not in digital I/O)							
	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
Low Leakage Input only	—	—	—	—	—	—	< 60pA (tested to 50nA)	< 60pA (tested to 50nA)
ADC	—	—	—	—	AN3	AN2	AN1	AN0
Op Amp	—	—	—	—	—	—	OPA- Input	OPA+ Input
VREF Inputs	—	—	—	—	VREF2 Input	VREF1 Input	—	—
Timer0	—	—	—	T0CKI	—	—	—	—
Timer1	T1CKI	—	—	—	—	—	—	—
Oscillator	OSC1/CLKIN	OSC2/CLKOUT	—	—	—	—	—	—
Reset	—	—	MCLR	—	—	—	—	—
Programming	—	—	Vpp	—	—	—	—	—

**Note 1:** Dashed cell implies that the Alternate Function does not apply.

TABLE 2B

Alternate Function	PORTB (when not in digital I/O)							
	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
INT	—	—	—	—	—	—	—	INT
ADC	—	—	—	—	AN7	AN6	AN5	AN4
Op amp	—	—	—	—	OPA Output	—	—	—
C2 comparator	C2 Output	—	—	—	AN7	AN6	AN5	AN4
C1 comparator	—	C1 Output	—	—	AN7	AN6	AN5	AN4
VREF Reference	—	—	—	—	—	—	—	VREF Output
DAC	—	—	—	—	—	—	—	VDAC Output
PSMC	PSMC1B Output	PSMC1A Output	—	—	—	—	—	—
Timer1	T1G Input	—	—	—	—	—	—	—
Programming	Data	Clock	—	—	—	—	—	—

**Note 1:** Dashed cell implies that the Alternate Function does not apply.

Figure 1 consists of 12 histograms arranged in a single column. Each histogram represents the frequency distribution of the number of non-zero elements in the vector  $x$  for a specific value of  $n$ . The x-axis for all histograms is 'Number of non-zero elements in  $x$ ' with major ticks at 0, 20, 40, 60, 80, 100, and 120. The y-axis is 'Frequency' with major ticks at 0, 2, 4, 6, 8, and 10. The histograms are labeled with  $n$  values: 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, and 120. As  $n$  increases, the distribution becomes more concentrated around  $n$ , and the peak frequency increases.

L'Espresso	
1980	100
1981	100
1982	100
1983	100
1984	100
1985	100
1986	100
1987	100
1988	100
1989	100
1990	100
1991	100
1992	100
1993	100
1994	100
1995	100
1996	100
1997	100
1998	100
1999	100
2000	100
2001	100
2002	100
2003	100
2004	100
2005	100
2006	100
2007	100
2008	100
2009	100
2010	100
2011	100
2012	100
2013	100
2014	100
2015	100
2016	100
2017	100
2018	100
2019	100
2020	100
2021	100
2022	100
2023	100
2024	100
2025	100
2026	100
2027	100
2028	100
2029	100
2030	100
2031	100
2032	100
2033	100
2034	100
2035	100
2036	100
2037	100
2038	100
2039	100
2040	100
2041	100
2042	100
2043	100
2044	100
2045	100
2046	100
2047	100
2048	100
2049	100
2050	100
2051	100
2052	100
2053	100
2054	100
2055	100
2056	100
2057	100
2058	100
2059	100
2060	100
2061	100
2062	100
2063	100
2064	100
2065	100
2066	100
2067	100
2068	100
2069	100
2070	100
2071	100
2072	100
2073	100
2074	100
2075	100
2076	100
2077	100
2078	100
2079	100
2080	100
2081	100
2082	100
2083	100
2084	100
2085	100
2086	100
2087	100
2088	100
2089	100
2090	100
2091	100
2092	100
2093	100
2094	100
2095	100
2096	100
2097	100
2098	100
2099	100
2100	100
2101	100
2102	100
2103	100
2104	100
2105	100
2106	100
2107	100
2108	100
2109	100
2110	100
2111	100
2112	100
2113	100
2114	100
2115	100
2116	100
2117	100
2118	100
2119	100
2120	100
2121	100
2122	100
2123	100
2124	100
2125	100
2126	100
2127	100
2128	100
2129	100
2130	100
2131	100
2132	100
2133	100
2134	100
2135	100
2136	100
2137	100
2138	100
2139	100
2140	100
2141	100
2142	100
2143	100
2144	100
2145	100
2146	100
2147	100
2148	100
2149	100
2150	100
2151	100
2152	100
2153	100
2154	100
2155	100
2156	100
2157	100
2158	100
2159	100
2160	100
2161	100
2162	100
2163	100
2164	100
2165	100
2166	100
2167	100
2168	100
2169	100
2170	100
2171	100
2172	100
2173	100
2174	100
2175	100
2176	100
2177	100
2178	100
2179	100
2180	100
2181	100
2182	100
2183	100
2184	100
2185	100
2186	100
2187	100
2188	100
2189	100
2190	100
2191	100
2192	100
2193	100
2194	100
2195	100
2196	100
2197	100
2198	100
2199	100
2200	100
2201	100
2202	100
2203	100
2204	100
2205	100
2206	100
2207	100
2208	100
2209	100
2210	100
2211	100
2212	100
2213	100
2214	100
2215	100
2216	100
2217	100
2218	100
2219	100
2220	100
2221	100
2222	100
2223	100
2224	100
2225	100
2226	100
2227	100
2228	100
2229	100
2230	100
2231	100
2232	100
2233	100
2234	100
2235	100
2236	100
2237	100
2238	100
2239	100
2240	100
2241	100
2242	100
2243	100
2244	100
2245	100
2246	100
2247	100
2248	100
2249	100
2250	100
2251	100
2252	100
2253	100
2254	100
2255	100
2256	100
2257	100
2258	100
2259	100
2260	100
2261	100
2262	100
2263	100
2264	100
2265	100
2266	100
2267	100
2268	100
2269	100
2270	100
2271	100
2272	100
2273	100
2274	100
2275	100
2276	100
2277	100
2278	100
2279	100
2280	100
2281	100
2282	100
2283	100
2284	100
2285	100
2286	100
2287	100
2288	100
2289	100
2290	100
2291	100
2292	100
2293	100
2294	100
2295	100
2296	100
2297	100
2298	100
2299	100
2300	100
2301	100
2302	100
2303	100
2304	100
2305	100
2306	100
2307	100
2308	100
2309	100
2310	100
2311	100
2312	100
2313	100
2314	100
2315	100
2316	100
2317	100
2318	100
2319	100
2320	100
2321	100
2322	100
2323	100
2324	100
2325	100
2326	100
2327	100
2328	100
2329	100
2330	100
2331	100
2332	100
2333	100
2334	100
2335	100
2336	100
2337	100
2338	100
2339	100
2340	100
2341	100
2342	100
2343	100
2344	100
2345	100
2346	100
2347	100
2348	100
2349	100
2350	100
2351	100
2352	100
2353	100
2354	100
2355	100
2356	100
2357	100
2358	100
2359	100
2360	100
2361	100
2362	100
2363	100
2364	100
2365	100
2366	100
2367	100
2368	100
2369	100
2370	100
2371	100
2372	100
2373	100
2374	100
2375	100
2376	100
2377	100
2378	100
2379	100
2380	100
2381	100
2382	100
2383	100
2384	100
2385	100
2386	100
2387	100
2388	100
2389	100
2390	100
2391	100
2392	100
2393	100
2394	100
2395	100
2396	100
2397	100
2398	100
2399	100
2400	100
2401	100
2402	100
2403	100
2404	100
2405	100
2406	100
2407	100
2408	100
2409	100
2410	100
2411	100
2412	100
2413	100
2414	100
2415	100
2416	100
2417	100
2418	100
2419	100
2420	100
2421	100
2422	100
2423	100
2424	100
2425	100
2426	100
2427	100
2428	100
2429	100
2430	100
2431	100
2432	100
2433	100
2434	100
2435	100
2436	100
2437	100
2438	100
2439	100
2440	100
2441	100
2442	100
2443	100
2444	100
2445	100
2446	100
2447	100
2448	100
2449	100
2450	100
2451	100
2452	100
2453	100
2454	100
2455	100
2456	100
2457	100
2458	100
2459	100
2460	100
2461	100
2462	100
2463	100
2464	100
2465	100
2466	100
2467	100
2468	100
2469	100
2470	100
2471	100
2472	100
2473	100
2474	100
2475	100
2476	100
2477	100
2478	100
2479	100
2480	100
2481	100
2482	100
2483	100
2484	100
2485	100
2486	100
2487	100
2488	100
2489	100
2490	100
2491	100
2492	100
2493	100
2494	100
2495	100
2496	100
2497	100
2498	100
2499	100
2500	100

TABLE 3 (cont'd)

[illegible]

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
RA6/OSC2/CLKOUT	<p>Diagram illustrating the block circuitry for the RA6/OSC2/CLKOUT pin. The circuit includes an oscillator circuit (OSC1) connected to the pin through a Schmitt Trigger Input Buffer. The pin is also connected to a Data Latch (D, Q) and a TRIS Latch (D, Q). The Data Latch is controlled by WR PORTA and RD PORTA. The TRIS Latch is controlled by WR TRISA and RD TRISA. The pin output is also connected to an INTRC or RC with CLKOUT block, which is controlled by INTRC or RC without CLKOUT. The pin is also connected to a Schmitt Trigger Input Buffer.</p>
RA7/OSC1/CLKIN	<p>Diagram illustrating the block circuitry for the RA7/OSC1/CLKIN pin. The circuit includes an oscillator circuit (OSC2) connected to the pin through a Schmitt Trigger Input Buffer. The pin is also connected to a Data Latch (D, Q) and a TRIS Latch (D, Q). The Data Latch is controlled by WR PORTA and RD PORTA. The TRIS Latch is controlled by WR TRISA and RD TRISA. The pin output is also connected to an INTRC or RC block, which is controlled by INTRC. The pin is also connected to a Schmitt Trigger Input Buffer.</p>

TABLE 3 (cont'd)

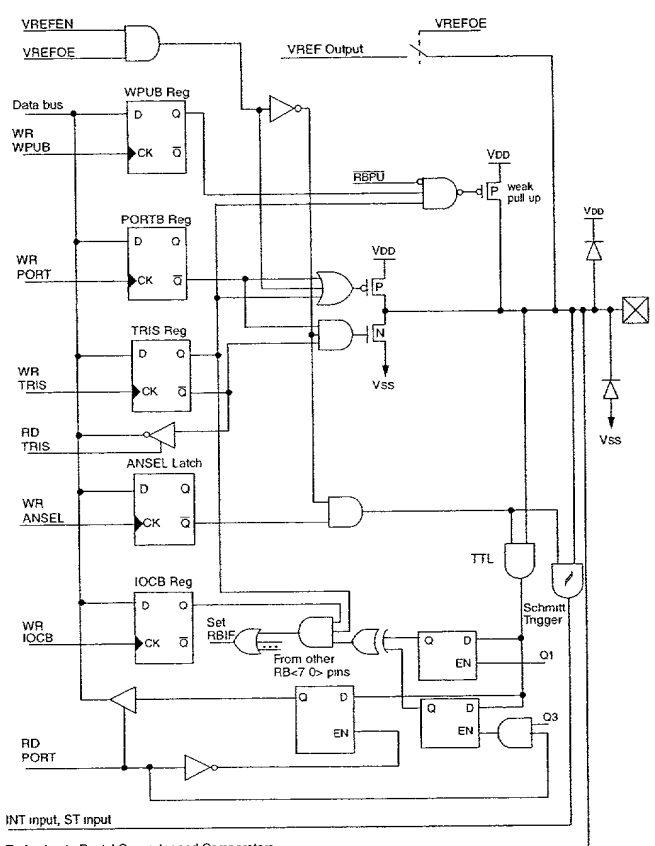
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB0/INT/AN4/VREF</p>	 <p>INT input, ST input</p> <p>To Analog to Digital Converter and Comparators</p>

TABLE 3 (cont'd)

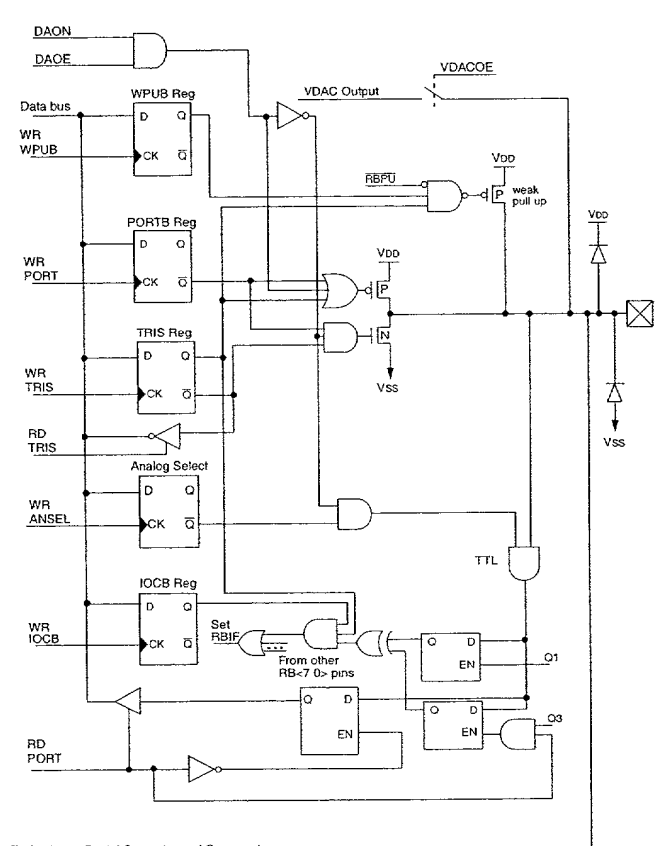
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB1/AN5/VDAC</p>	 <p>To Analog to Digital Converter and Comparators</p>

TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB2/AN6</p>	<p>The diagram illustrates the internal circuitry for the RB2/AN6 pin. It shows the following components and connections:</p> <ul style="list-style-type: none"> <li><b>Registers:</b> WPUB Reg, PORTB Reg, TRIS Reg, ANSEL Latch, and IOCB Reg. Each register has a Data bus input, a Write (WR) or Read (RD) control input, and a Clock (CK) input.</li> <li><b>Weak Pull-up:</b> A pull-up resistor connected to VDD, labeled "weak pull-up".</li> <li><b>TTL Input:</b> A TTL input signal connected to the pin.</li> <li><b>Diode Network:</b> A network of diodes connected to VDD and VSS, used for signal conditioning.</li> <li><b>Analog-to-Digital Converter:</b> The output of the pin is connected to the input of an Analog-to-Digital Converter.</li> <li><b>Control Signals:</b> The circuit is controlled by various signals including Data bus, WR, RD, and PORT.</li> </ul>

TABLE 3 (cont'd)

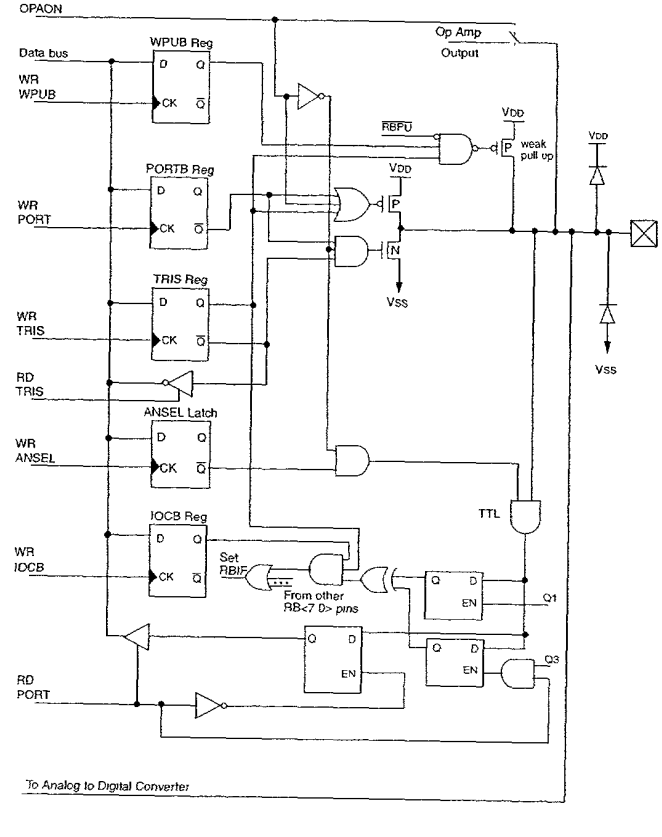
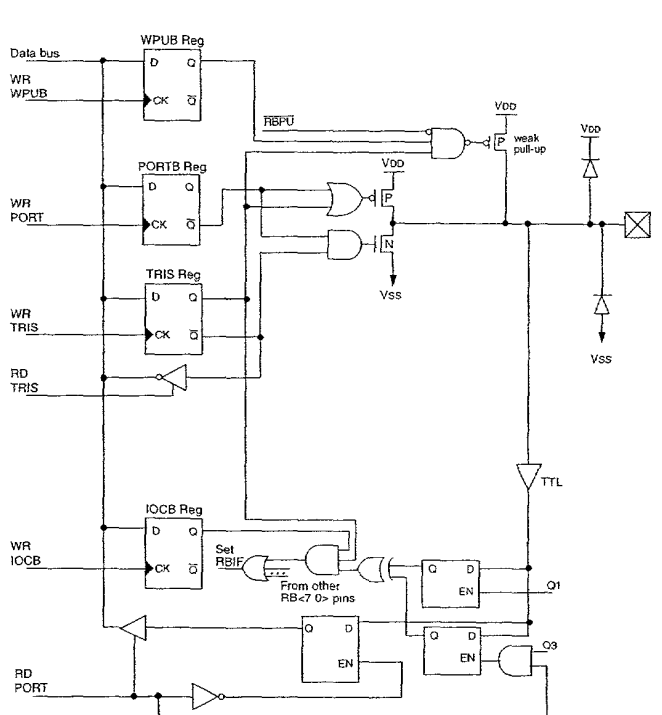
PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p data-bbox="334 634 438 661">RB3/AN7/OPA</p>	 <p data-bbox="712 1041 883 1066">To Analog to Digital Converter</p>
<p data-bbox="319 1440 425 1465">RB4 AND RB5</p>	

TABLE 3 (cont'd)

PIN NAME

EXEMPLARY BLOCK CIRCUITRY

RB6/C1/PSMC1A

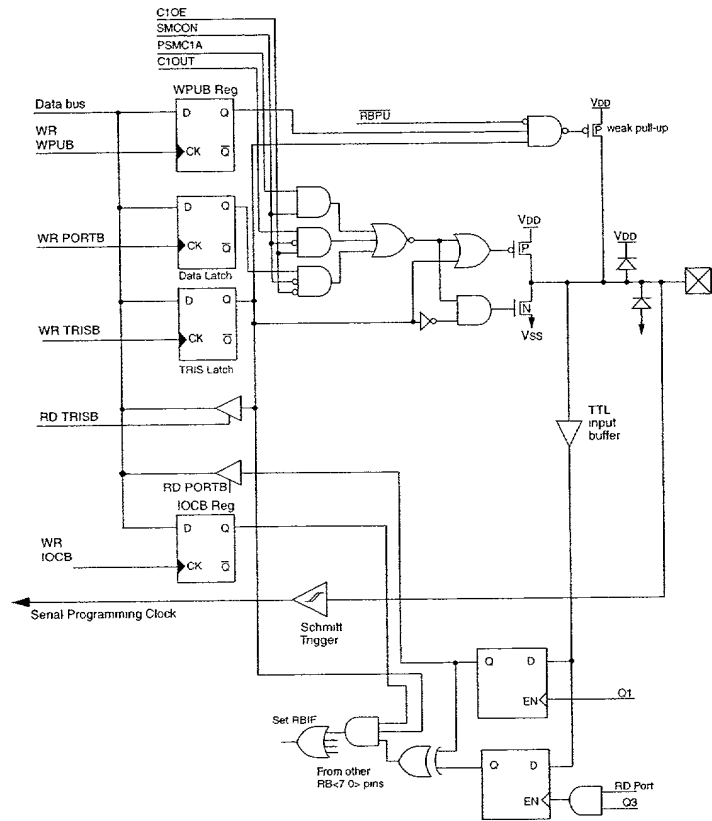
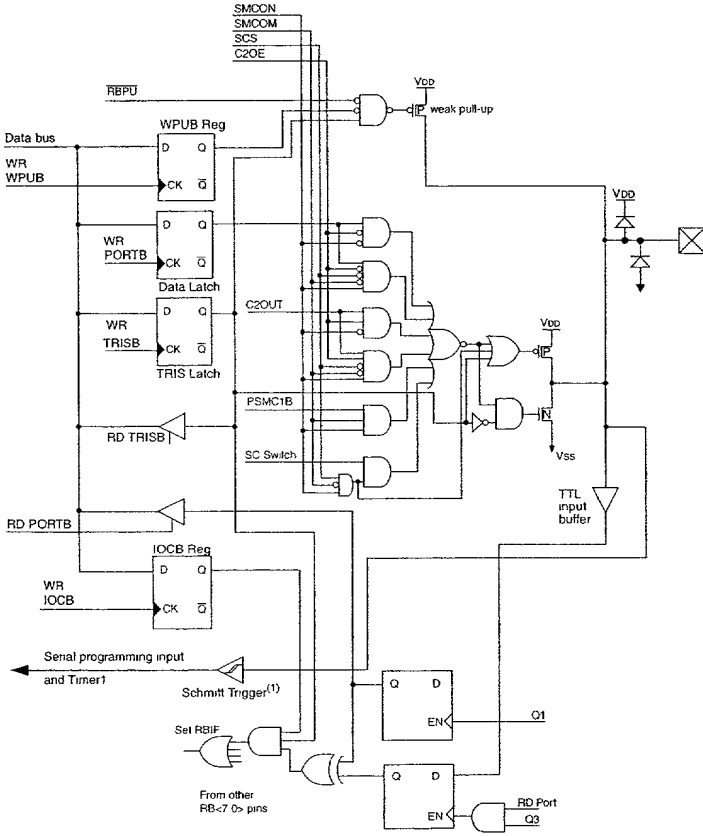


TABLE 3 (cont'd)

PIN NAME	EXEMPLARY BLOCK CIRCUITRY
<p>RB7/C2/PSMC1B/T1G</p>	 <p>The diagram illustrates the internal block circuitry for the pin RB7/C2/PSMC1B/T1G. It shows the connection of the pin to the data bus (WR, WPU, RD, PORTB, TRISB, IOCB) and the output driver (C2OUT, SC Switch, PSMC1B, C1, Q1, Q3). The circuit includes several registers (WPUB Reg, PORTB, TRISB, IOCB Reg) and latches (Data Latch, TRIS Latch). It also shows the connection to the data bus (WR, WPU, RD, PORTB, TRISB, IOCB) and the output driver (C2OUT, SC Switch, PSMC1B, C1, Q1, Q3). The circuit includes several registers (WPUB Reg, PORTB, TRISB, IOCB Reg) and latches (Data Latch, TRIS Latch). It also shows the connection to the data bus (WR, WPU, RD, PORTB, TRISB, IOCB) and the output driver (C2OUT, SC Switch, PSMC1B, C1, Q1, Q3). The circuit includes several registers (WPUB Reg, PORTB, TRISB, IOCB Reg) and latches (Data Latch, TRIS Latch). It also shows the connection to the data bus (WR, WPU, RD, PORTB, TRISB, IOCB) and the output driver (C2OUT, SC Switch, PSMC1B, C1, Q1, Q3).</p>